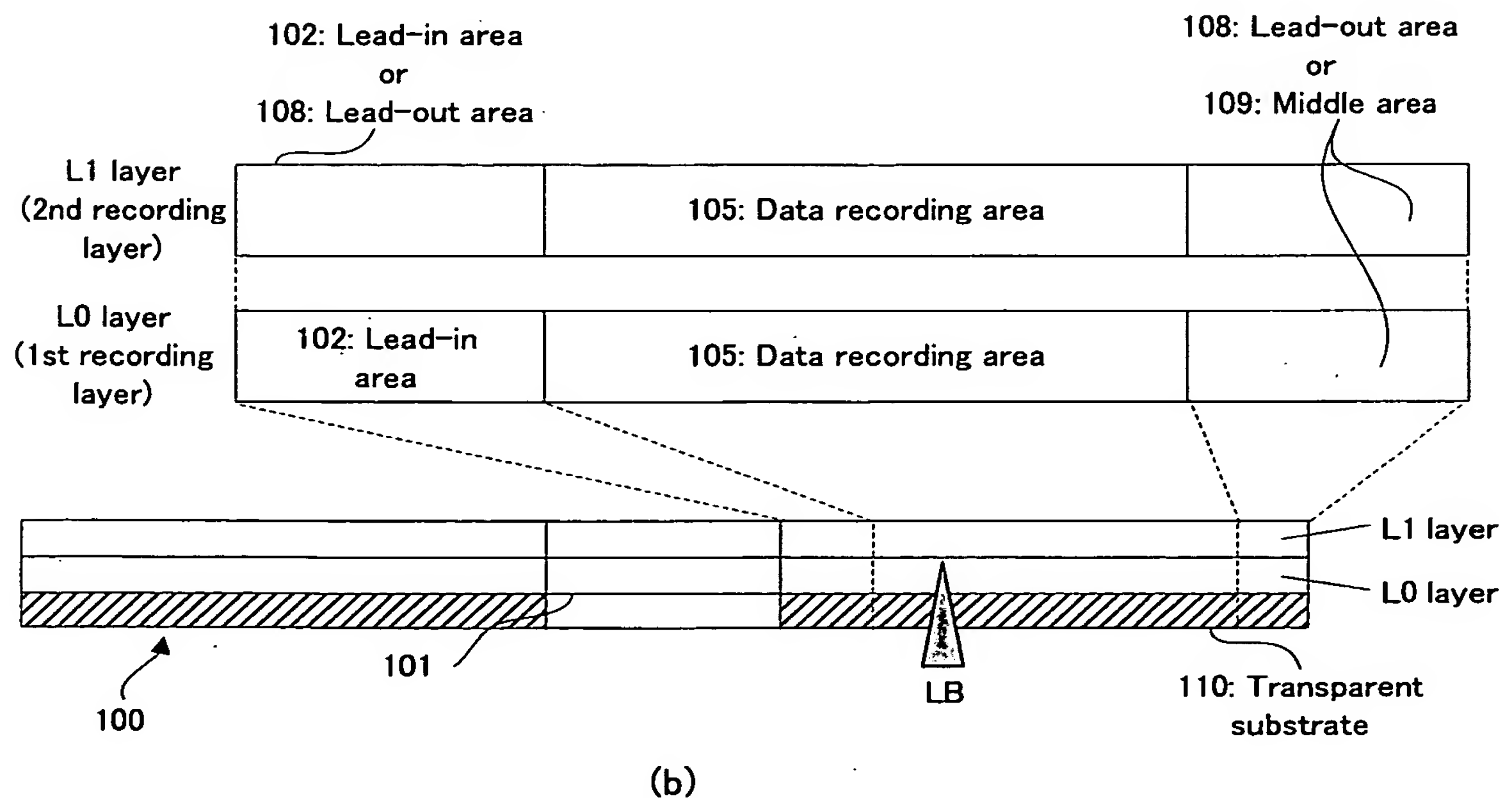
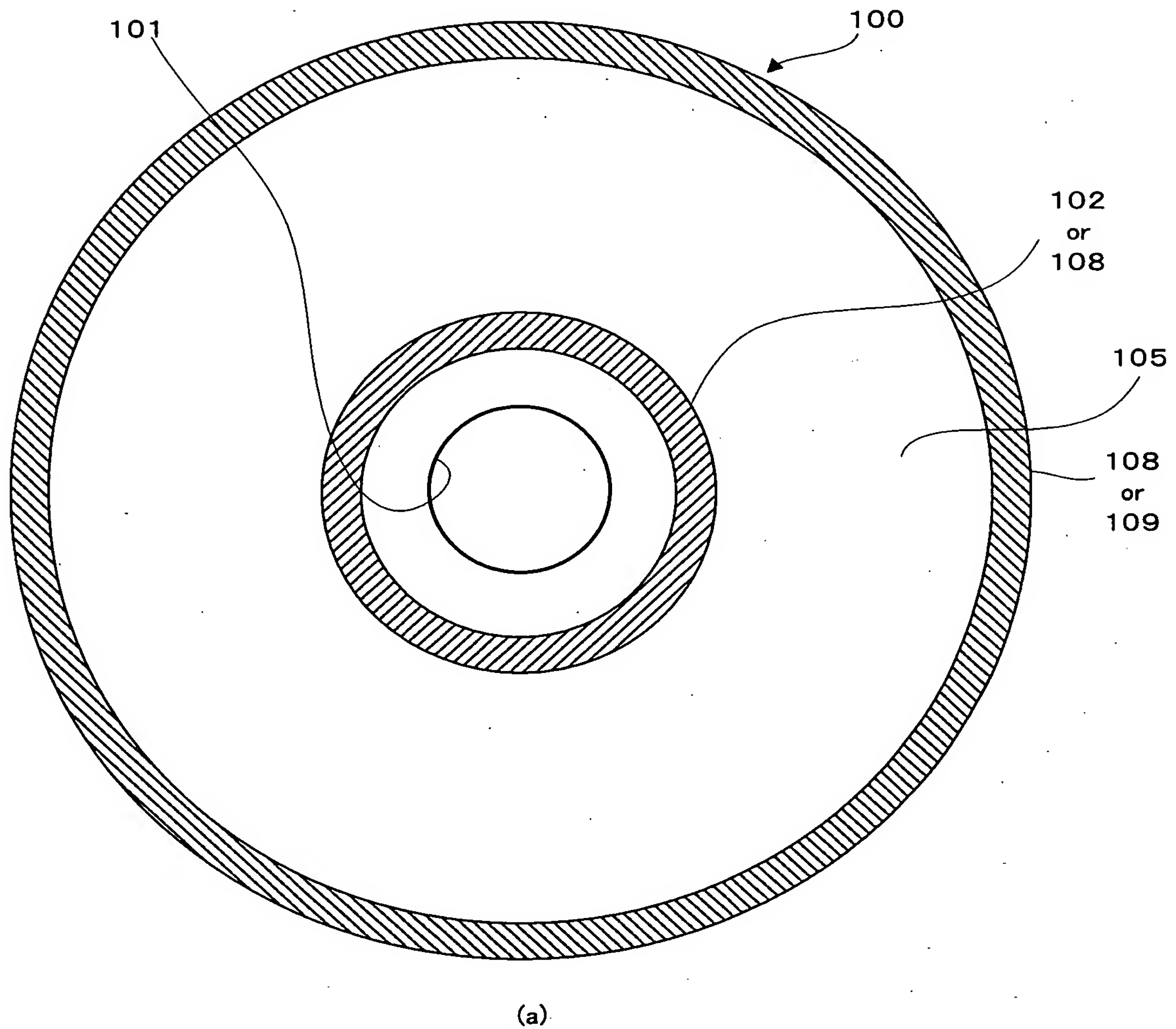


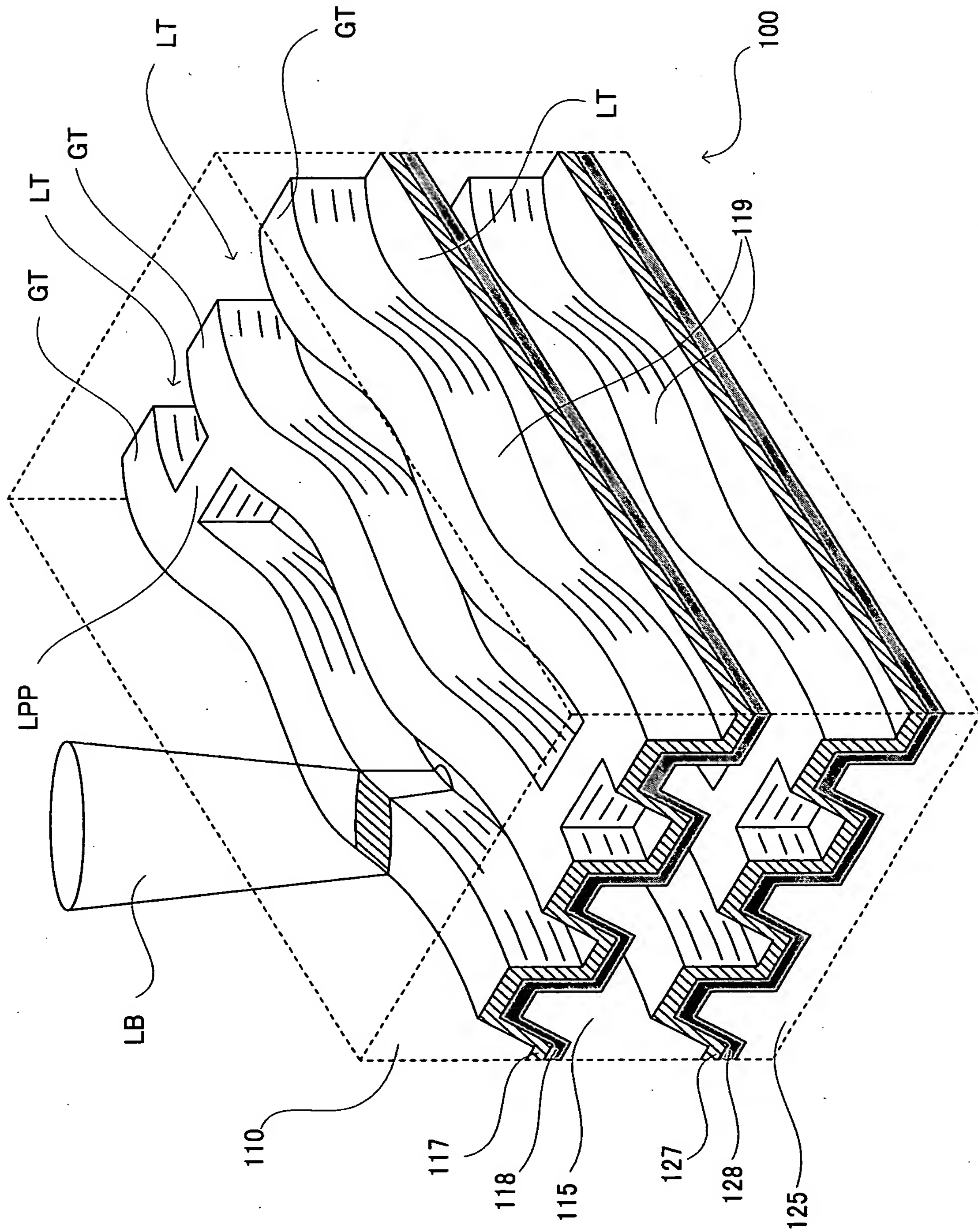
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[FIG. 1]

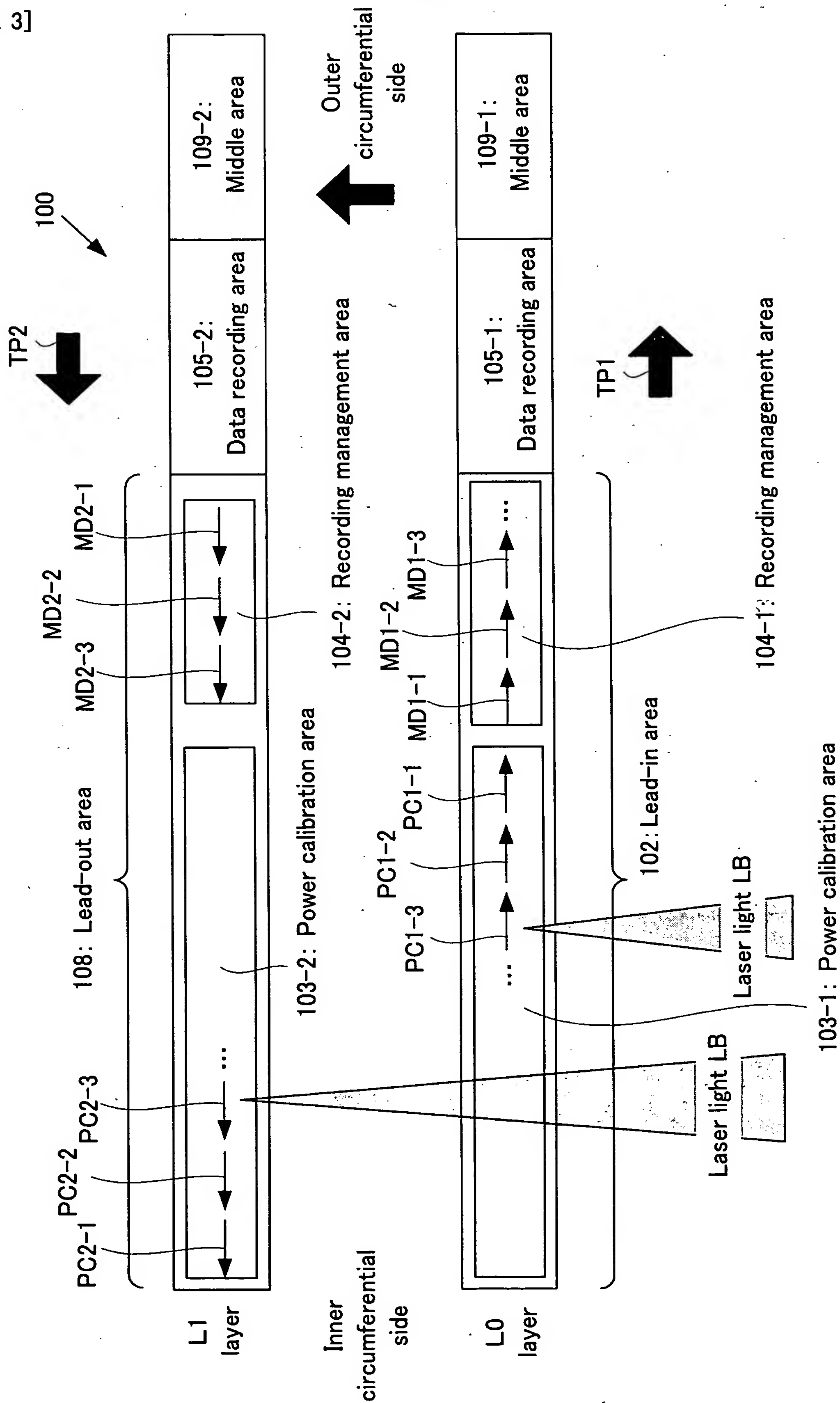


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[FIG. 2]



[FIG. 3]



The diagram illustrates a cross-sectional view of a multi-layered structure, likely a semiconductor device, divided into two main horizontal sections: the **L1 layer** (top) and the **L0 layer** (bottom).

L1 layer details:

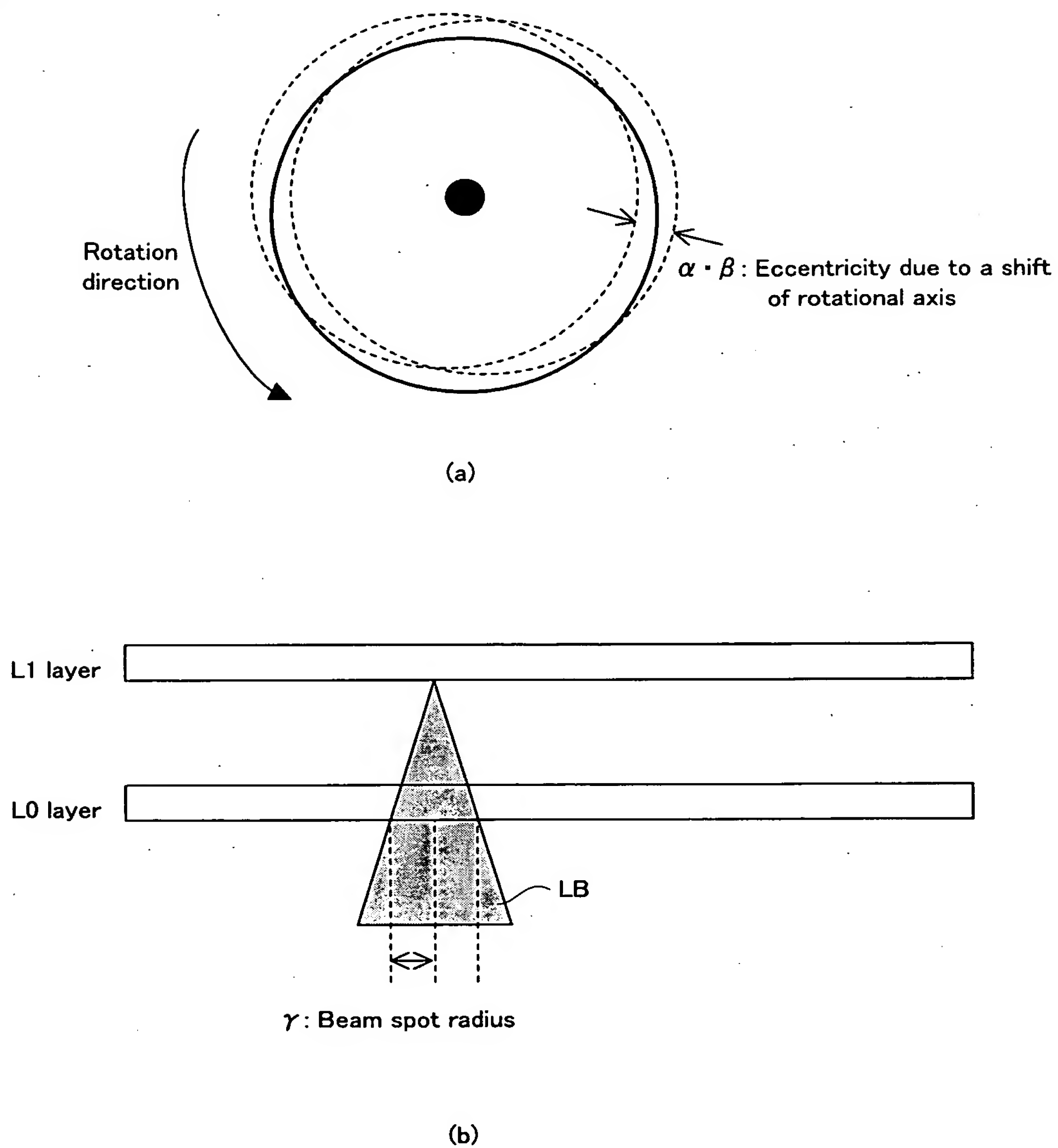
- The left portion of the L1 layer is labeled **103-2** and contains a region with a cross-hatch pattern labeled **103U-2**.
- The right portion of the L1 layer is labeled **103-1** and contains a region with a diagonal hatch pattern labeled **103U-1**.
- Between these two regions is a central area labeled **103R-2**.
- Within the **103R-2** area, there are three sub-regions labeled **PC2-1**, **PC2-2**, and **PC2-3**, each indicated by a horizontal arrow pointing to the right.
- A dimension **D** is indicated by a double-headed arrow between the vertical boundaries of the **103U-1** and **103U-2** regions.

L0 layer details:

- The left portion of the L0 layer is labeled **103-2** and contains a region with a cross-hatch pattern labeled **103U-2**.
- The right portion of the L0 layer is labeled **103-1** and contains a region with a diagonal hatch pattern labeled **103U-1**.
- Between these two regions is a central area labeled **103R-1**.
- Within the **103R-1** area, there are three sub-regions labeled **PC1-1**, **PC1-2**, and **PC1-3**, each indicated by a horizontal arrow pointing to the right.
- A dimension **D** is indicated by a double-headed arrow between the vertical boundaries of the **103U-1** and **103U-2** regions.

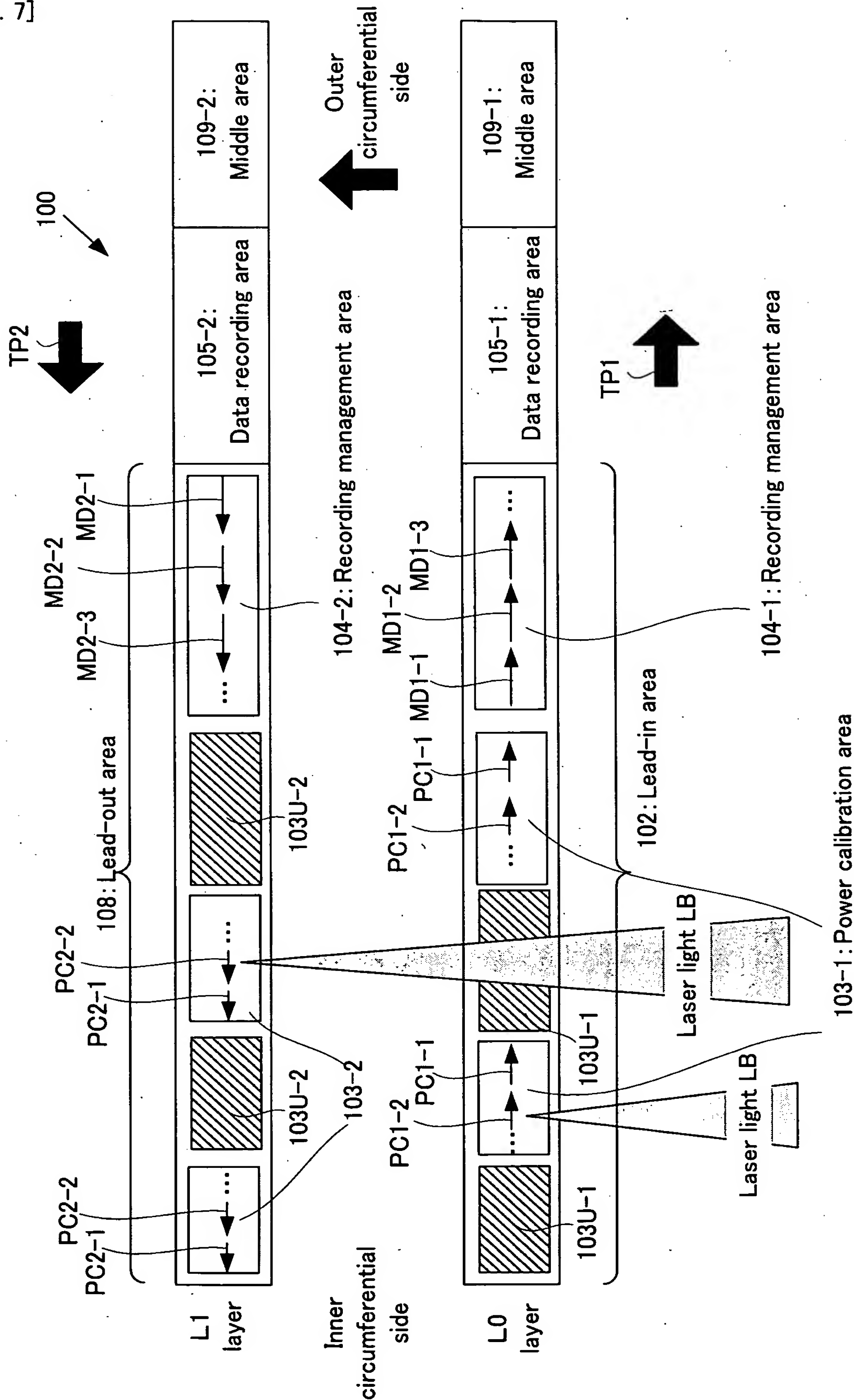
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[FIG. 5]



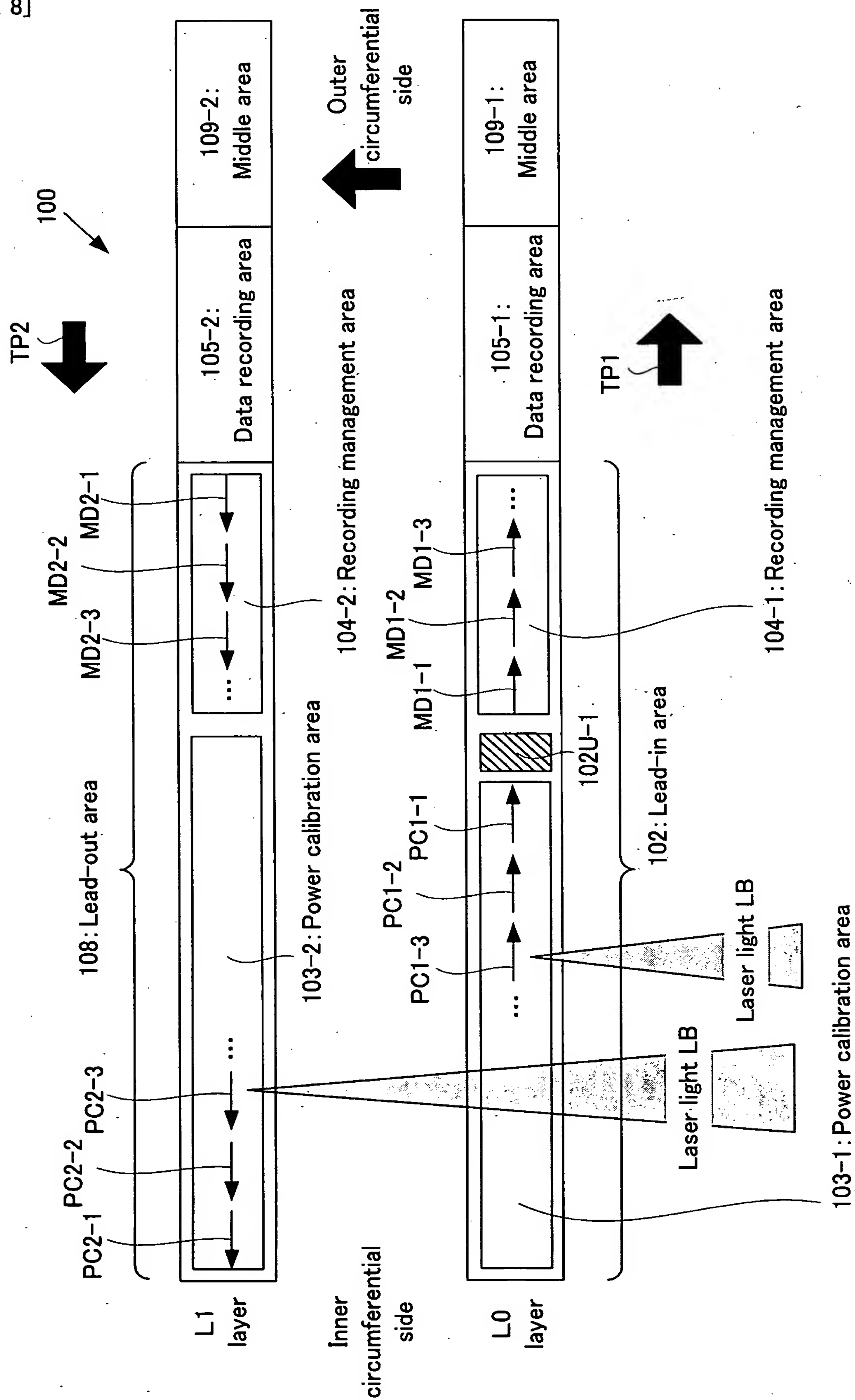
[illegible]

[FIG. 7]

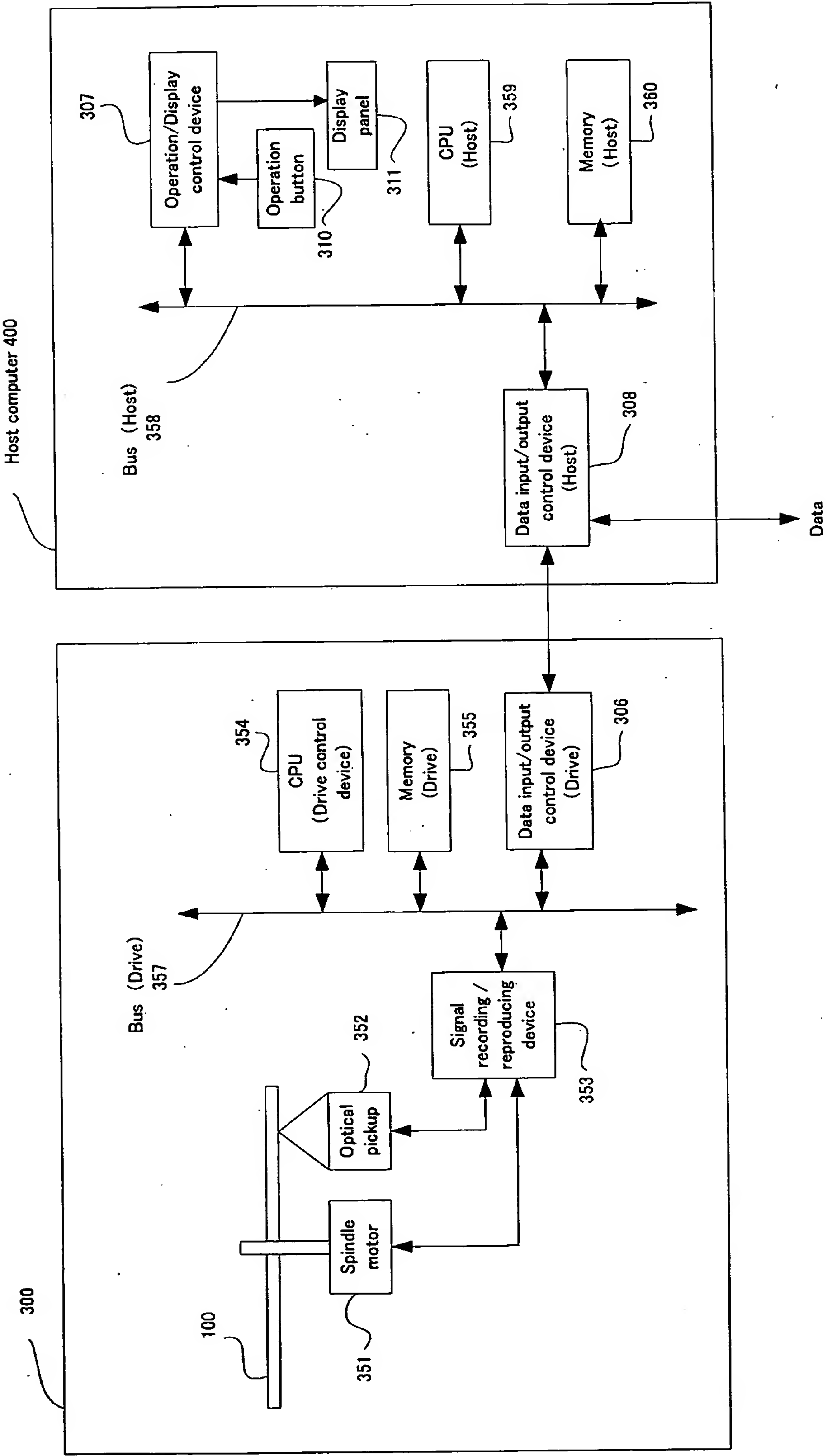


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[FIG. 8]

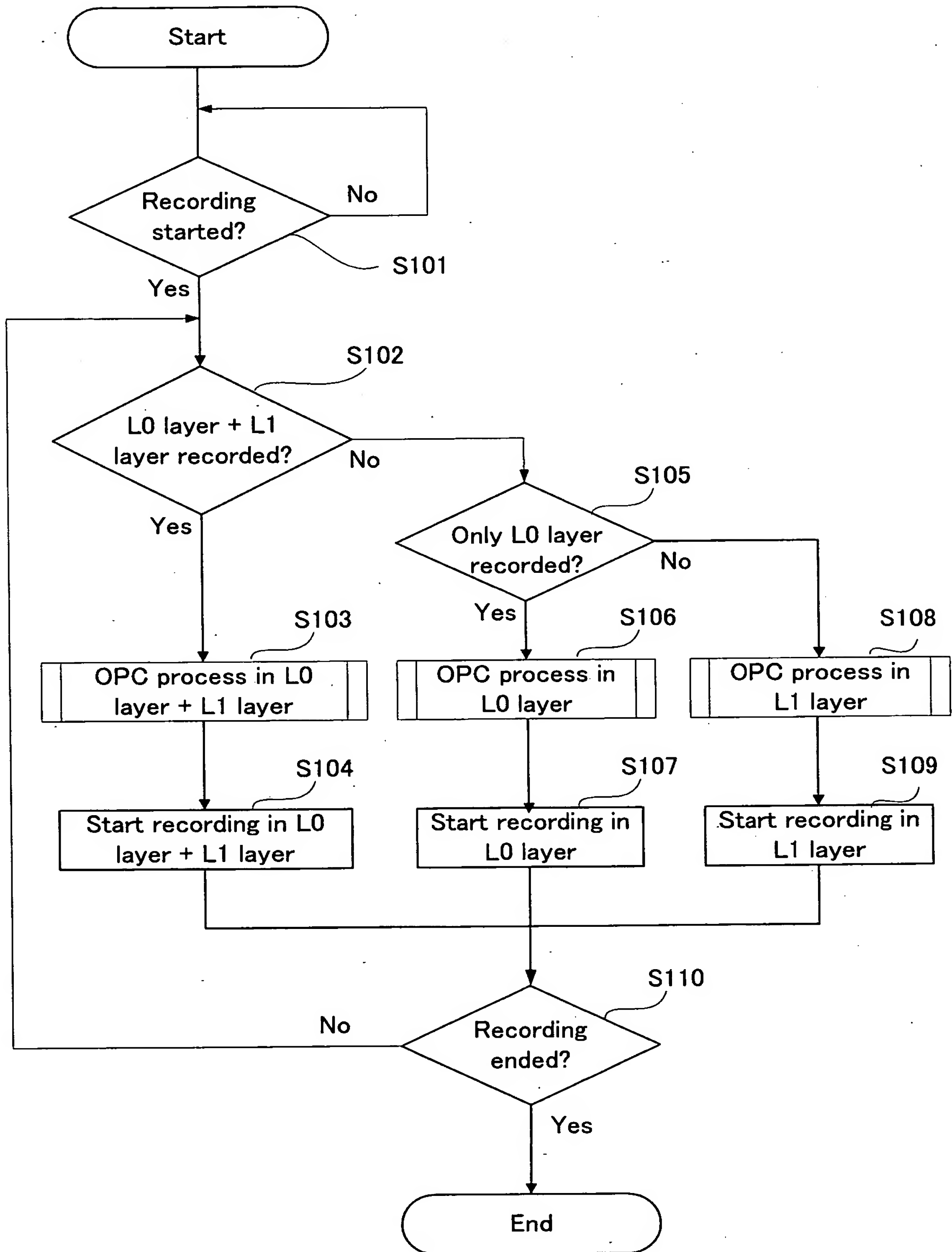


[FIG. 9]



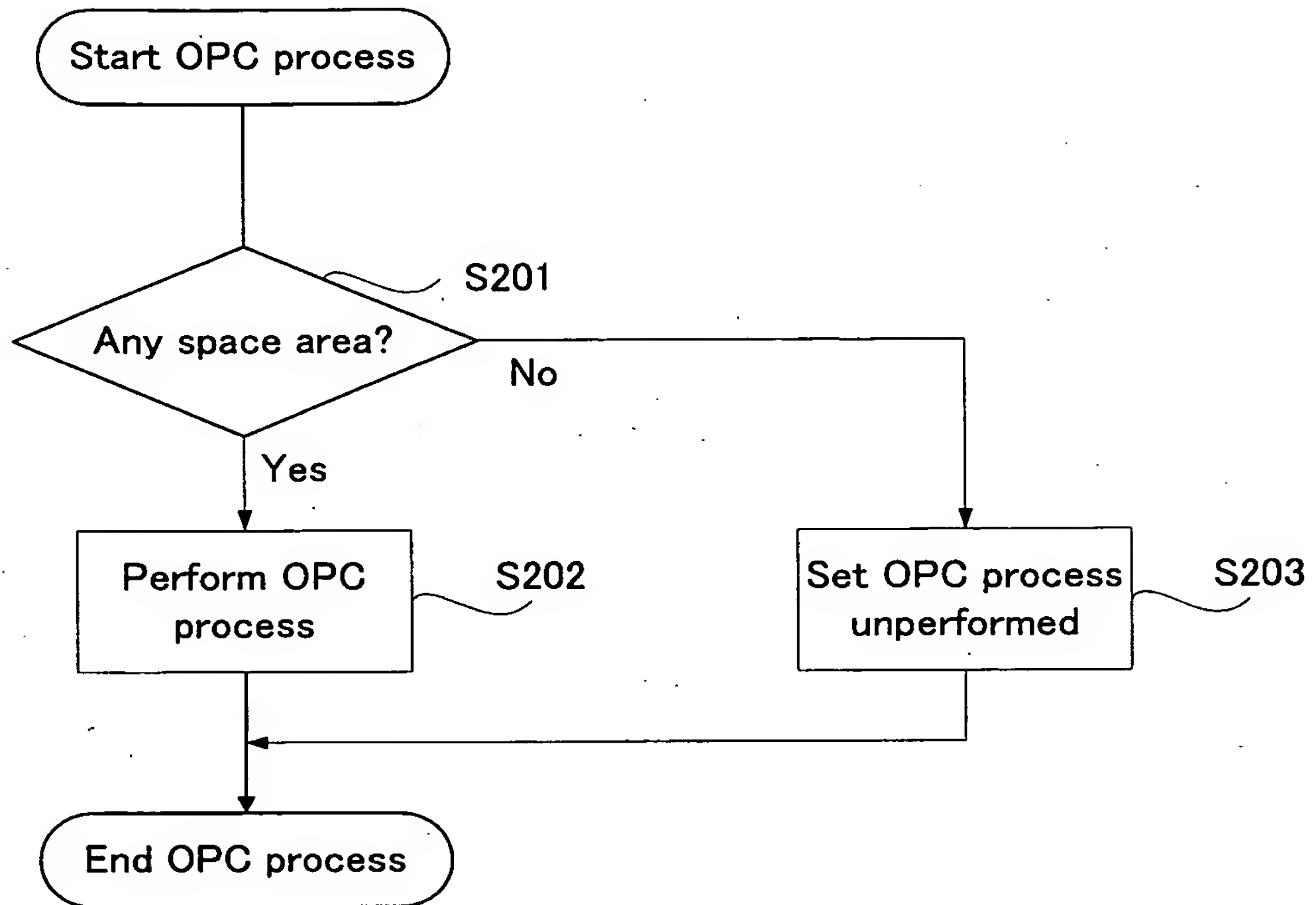
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[FIG. 10]



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[FIG. 11]



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[FIG. 12]

